
# 74LVC10A-Q100

## Triple 3-input NAND gate

Rev. 1 — 24 January 2024 Product data sheet

## 1. General description

The 74LVC10A-Q100 provides three 3-input NAND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC10APW-Q100 | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

nexperia

## 4. Functional diagram

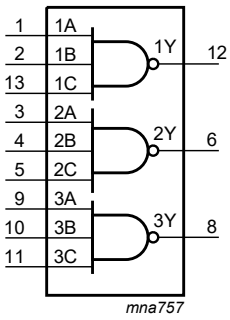



Fig. 1. Logic symbol

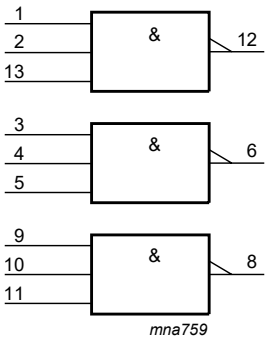



Fig. 2. IEC logic symbol

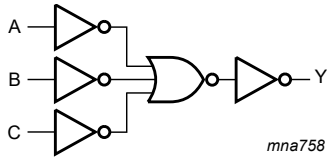
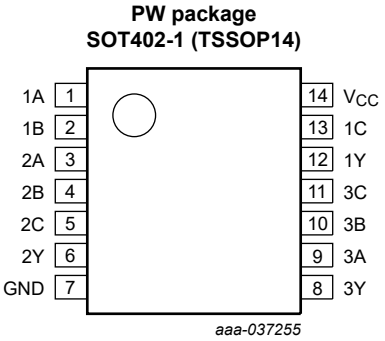



Fig. 3. Logic diagram (one gate)

## 5. Pinning information

### 5.1. Pinning




### 5.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1A, 2A, 3A | 1, 3, 9 | data input |
| 1B, 2B, 3B | 2, 4, 10 | data input |
| 1C, 2C, 3C | 13, 5, 11 | data input |
| 1Y, 2Y, 3Y | 12, 6, 8 | data output |
| GND | 7 | ground (0 V) |
| $V_{CC}$ | 14 | supply voltage |

# 6. Functional description

**Table 3. Function selection**

*H = HIGH voltage level; L = LOW voltage level; X = don't care*

| Input | | | Output |
|---|---|---|---|
| **nA** | **nB** | **nC** | **nY** |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |
| H | H | H | L |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | -50 | - | mA |
| $V_I$ | input voltage | [1] | -0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| $V_O$ | output voltage | [2] | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | - | ±50 | mA |
| $I_{CC}$ | supply current | | - | 100 | mA |
| $I_{GND}$ | ground current | | -100 | - | mA |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C [3] | - | 500 | mW |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT402-1 (TSSOP14) package: $P_{tot}$ derates linearly with 7.3 mW/K above 81 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | - | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | in free air | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | - | - | 0.65 × $V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 0.35 × $V_{CC}$ | - | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | - | - | $V_{CC}$ - 0.3 | - | V |
| | | $I_O$ = -4 mA; $V_{CC}$ = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | $I_O$ = -8 mA; $V_{CC}$ = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | $I_O$ = -18 mA; $V_{CC}$ = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | $I_O$ = -24 mA; $V_{CC}$ = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A | - | 0.1 | 10 | - | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 2.7 V to 3.6 V; $V_I$ = $V_{CC}$ - 0.6 V; $I_O$ = 0 A | - | 5 | 500 | - | 5000 | µA |
| $C_I$ | input capacitance | $V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND to $V_{CC}$ | - | 4.0 | - | - | - | pF |

[1] All typical values are measured at $V_{CC}$ = 3.3 V (unless stated otherwise) and $T_{amb}$ = 25 °C.

# 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nA, nB, nC to nY; see Fig. 4 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 13 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 0.5 | 4.5 | 11.2 | 0.5 | 12.9 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.7 | 6.3 | 1.0 | 7.4 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 2.8 | 6.7 | 1.5 | 7.8 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 2.4 | 5.7 | 1.5 | 6.6 | ns |
| $C_{PD}$ | power dissipation capacitance | per gate; $V_I$ = GND to $V_{CC}$ [3] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | 2.9 | - | - | - | pF |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | 6.0 | - | - | - | pF |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 8.8 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz

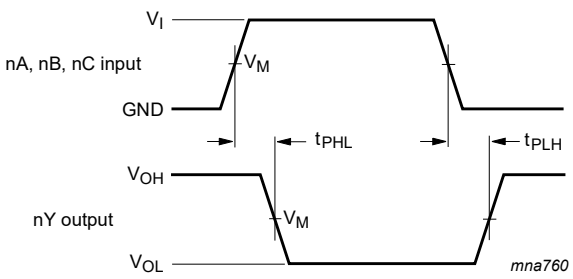
$C_L$ = output load capacitance in pF

$V_{CC}$ = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

## 10.1. Waveforms and test circuit

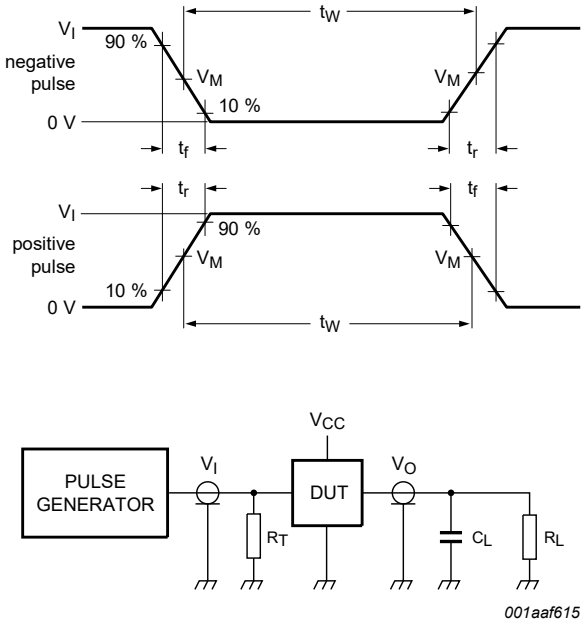



$V_M$ = 1.5 V at $V_{CC}$ ≥ 2.7 V

$V_M$ = 0.5 × $V_{CC}$ at $V_{CC}$ < 2.7 V.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 4. Input (nA, nB and nC) to output (nY) propagation delays**




Test data is given in Table 8. Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

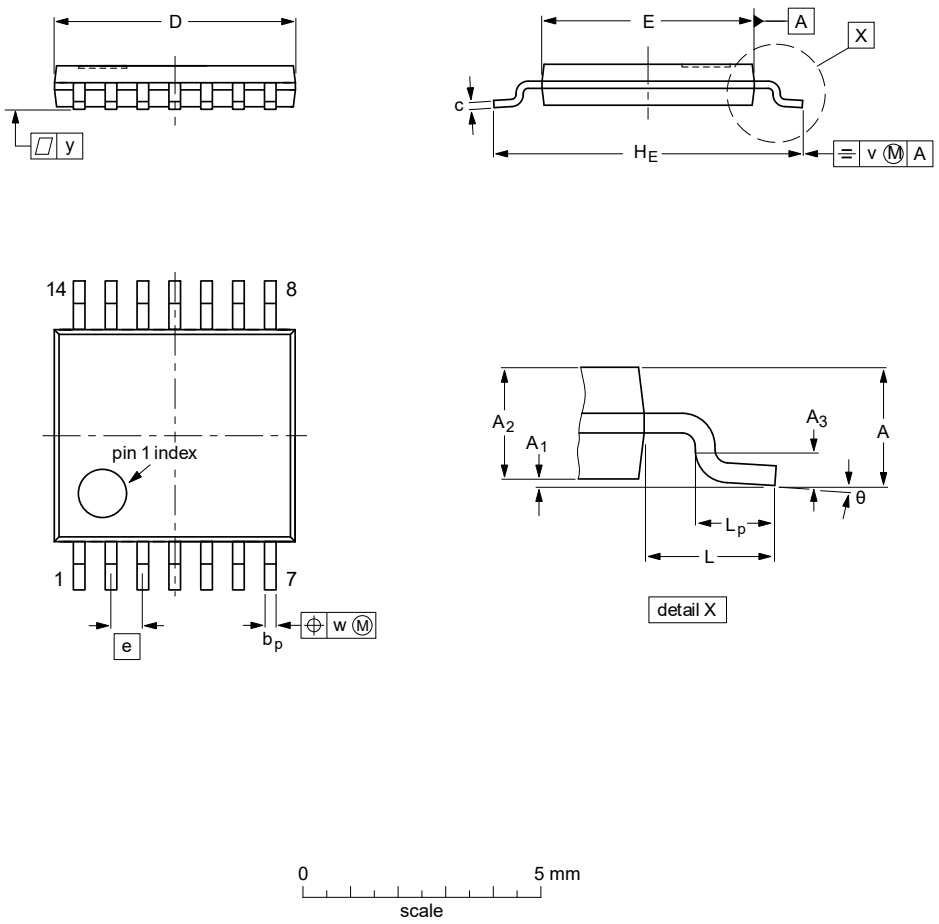
**Fig. 5. Test circuit for measuring switching times**

**Table 8. Test data**

| Supply voltage | Input | | Load | |
|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ |
| 1.2 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 500 Ω |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω |

## 11. Package outline

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.20 | 0.15 | 1.05 | | 0.30 | 0.2 | 5.1 | 4.5 | | 6.6 | | 0.75 | | | | 8° |
| | nom | | | | 0.25 | | | | | 0.65 | | 1 | | 0.2 | 0.1 | 0.1 | |
| | min | | 0.05 | 0.80 | | 0.19 | 0.09 | 4.9 | 4.3 | | 6.2 | | 0.45 | | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

*sot402-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~03-02-18~~ 23-10-27 |

**Fig. 6. Package outline SOT402-1 (TSSOP14)**

## 12. Abbreviations

**Table 9. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC10A_Q100 v.1 | 20240124 | Product data sheet | - | - |

# 14. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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**Date of release: 24 January 2024**